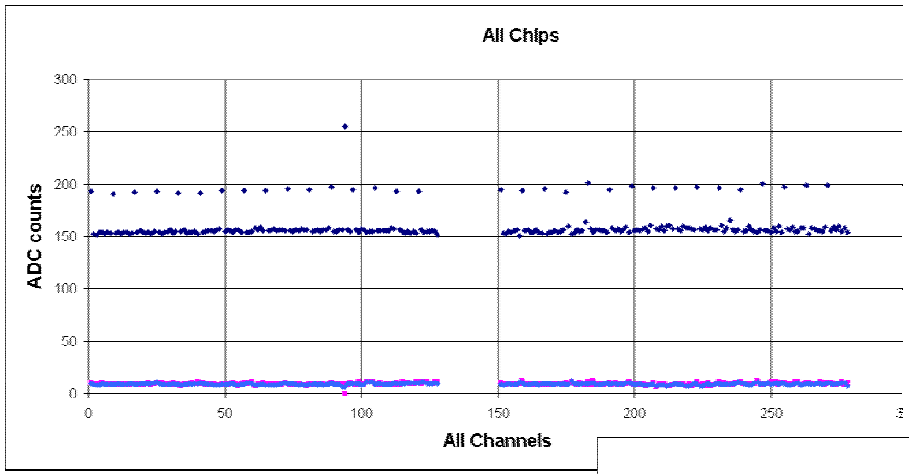
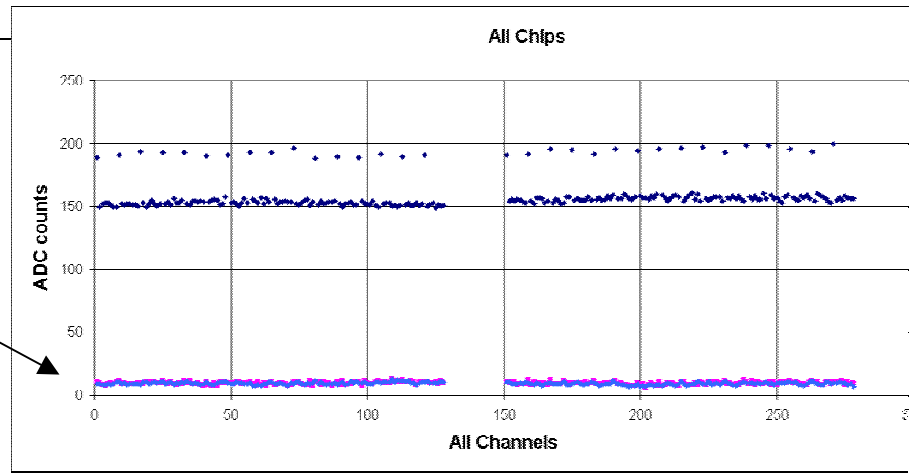
L0 Hybrid

- Two hybrids stuffed with version 1 (old) SVX4.

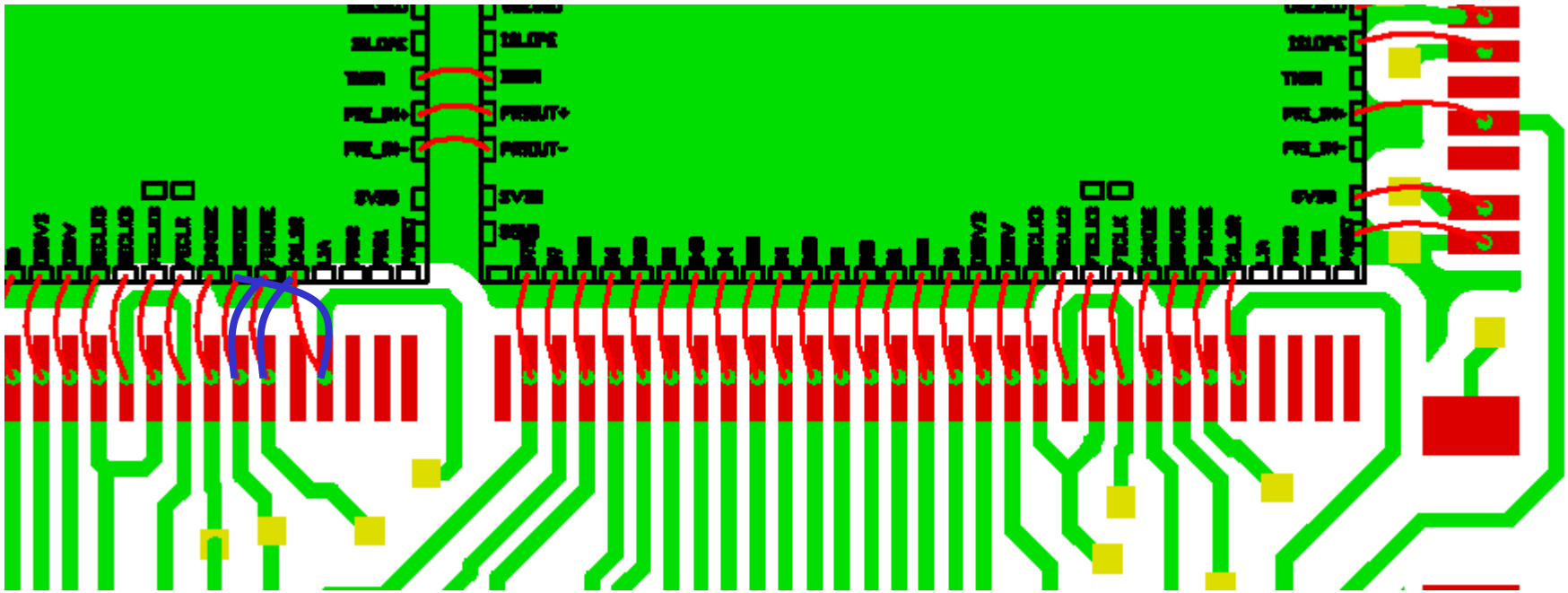


Noise level same as the other type of hybrids.



- Both work fine.

L0 Hybrid (cont'd)



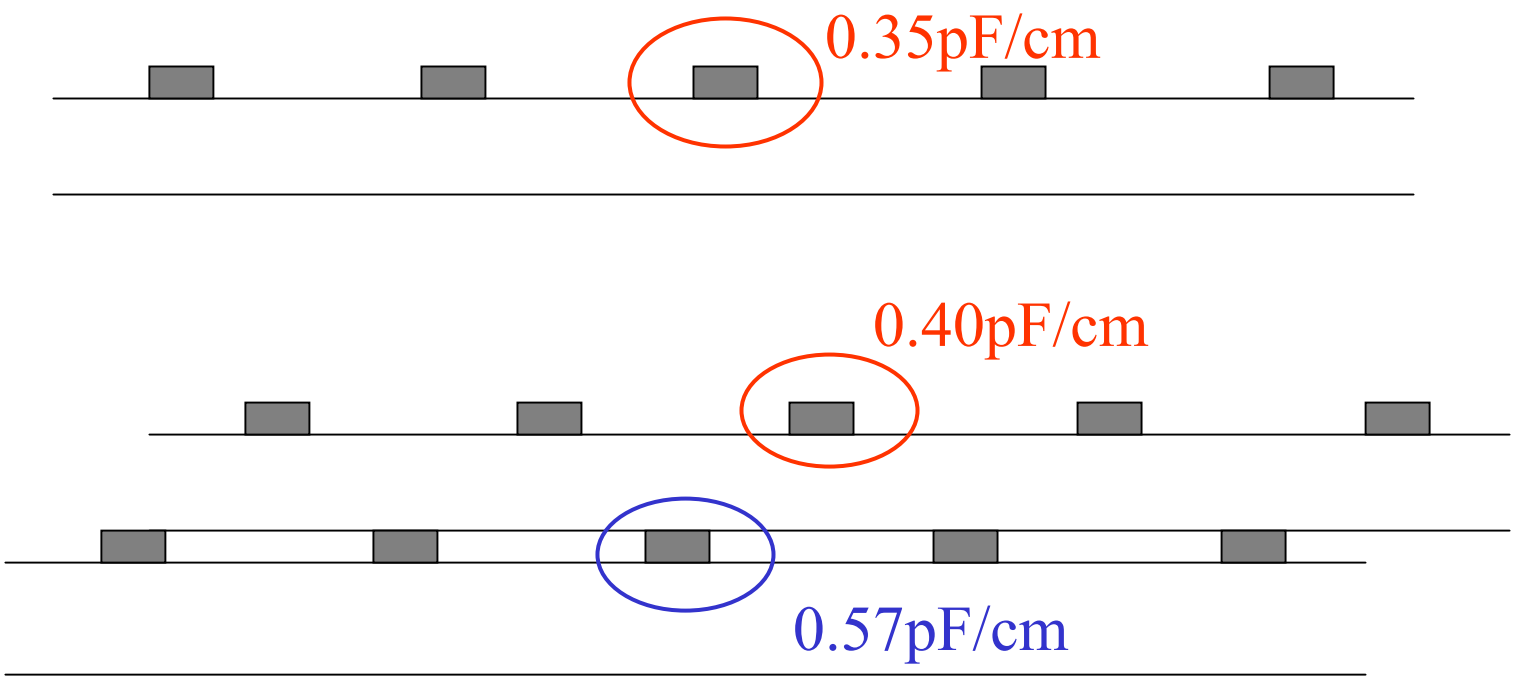
- Minor problem: FE mode, BE mode, and calsr are misaligned between 1st and 2nd chip.
- 1st chip calsr → 2nd chip FE mode
- 1st chip FE mode → 2nd chip BE mode
- 1st chip BE mode → 2nd chip calsr

@ Etch layer 2

- These are temporarily fixed by the wire bonding scheme.

Revised ANSYS calculation

- ANSYS calculation:
  91μm pitch, 16μm trace width, 8μm trace height, and 70μm Kapton thickness (was 50μm).



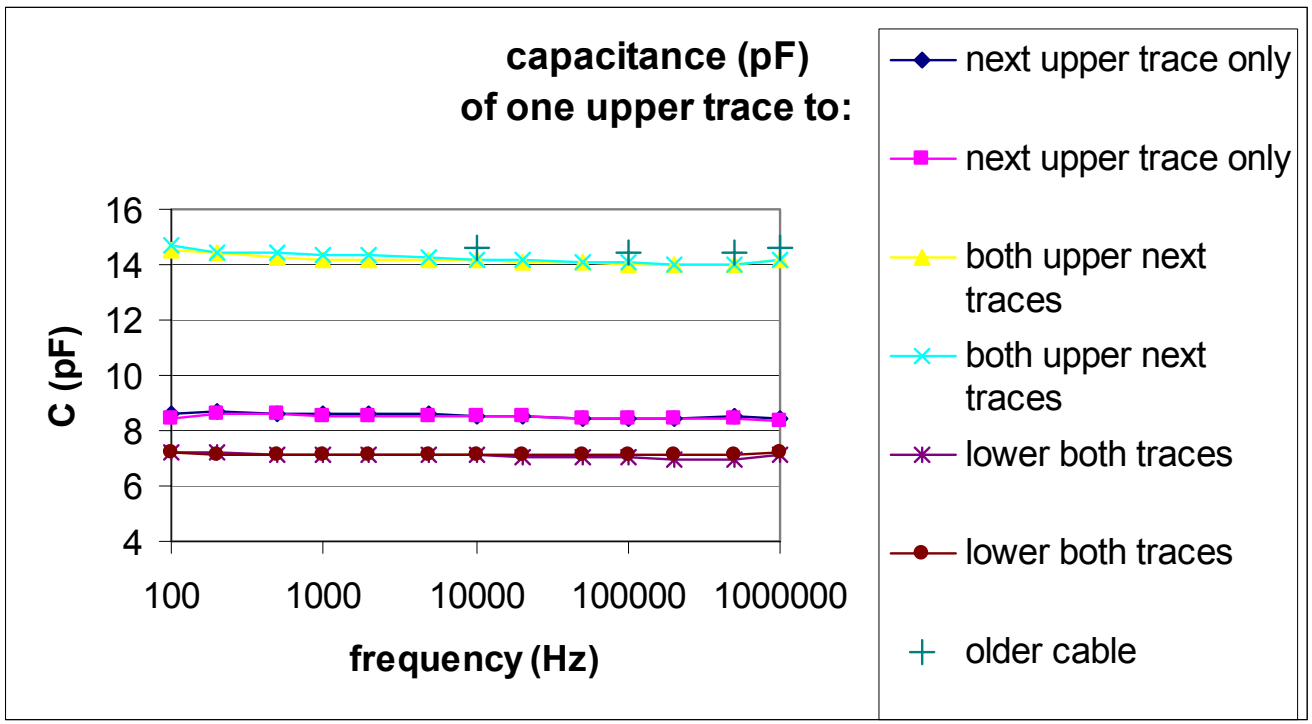
LCR measurement

- Neighbor to neighbor capacitance:
  7.5pF (single cable) → 8.5pF (top cable of the two stacked cable).
- 13% increase of capacitance is in good agreement with the ANSYS calculation.
- Frank also sees the noise increase for the laminated cable stack.

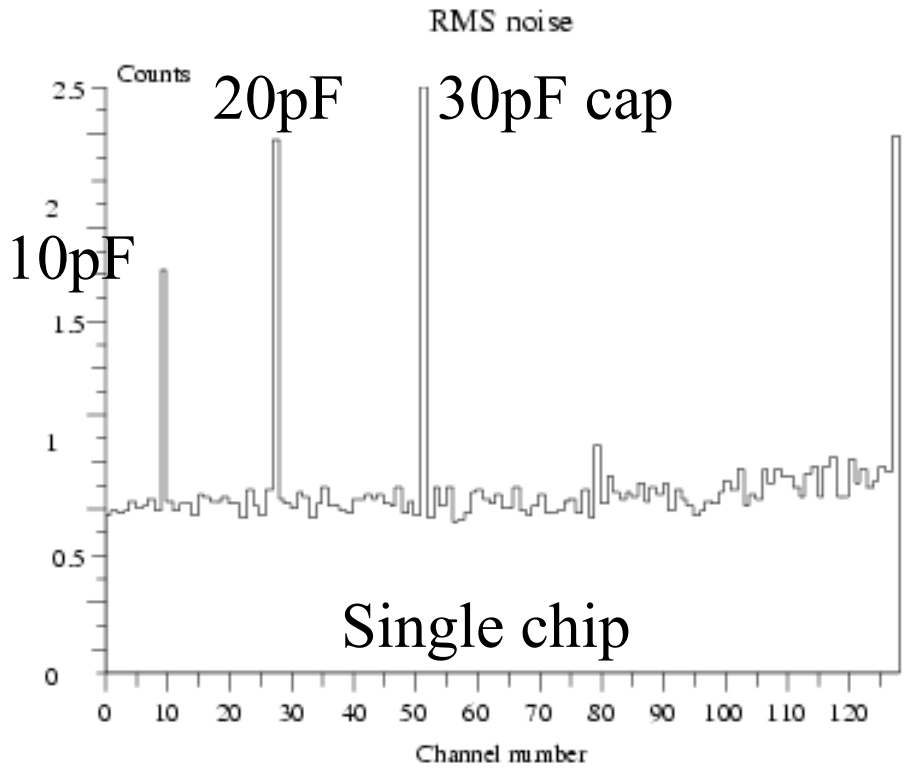
Frank's Slide

Short look at capacitances of cable assembly

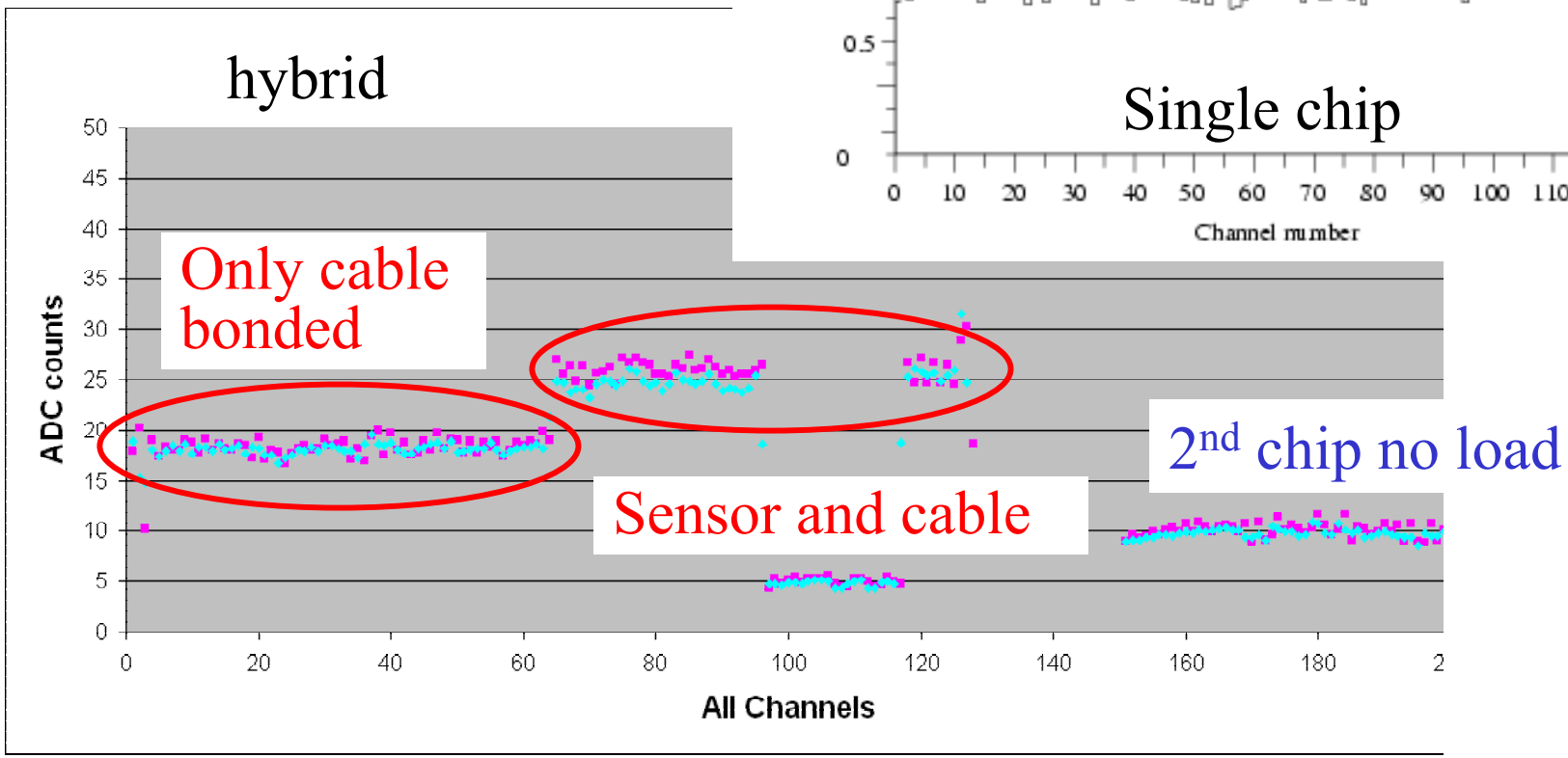
- 0.34 pF/cm averaged to both neighbors
- add 0.17 pF/cm to lower cable
- total cap: 0.51 pF/cm for cable stack plus ~10% for higher orders
- ANSYS calculation by Kazu: 0.47 pF/cm for 200um spacer with dielectric constant of 2.0 (we have ~2.5)



SVX4 sees capacitive load



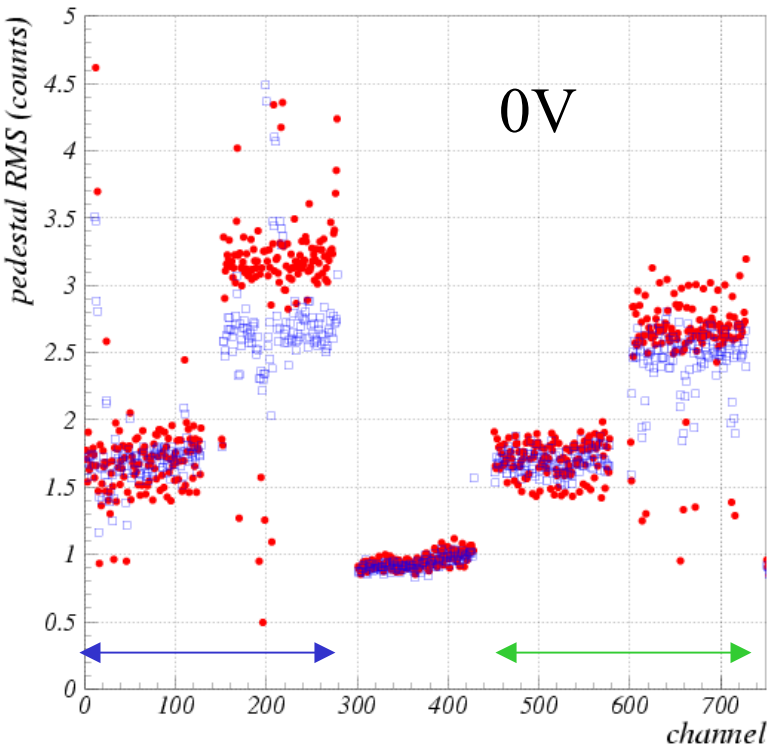
hybrid



New module with 10 chip hybrid

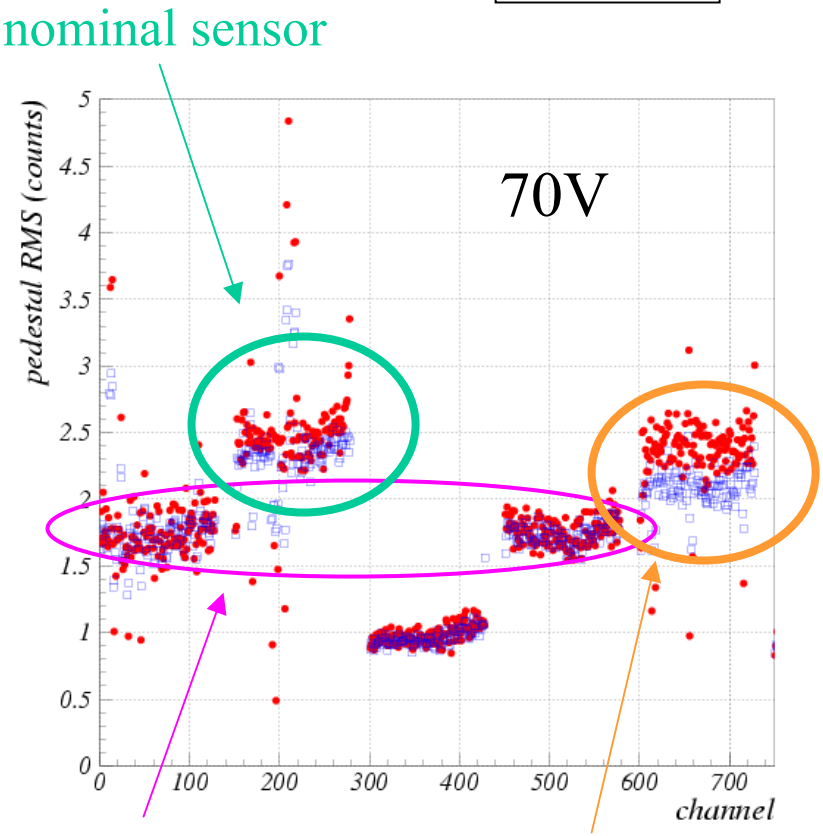
- Very useful for the cable studies.

BW=6



Pre-laminated by Dyconex

Nominal cables



cable only

very good cut sensor

Checking Gain

- Large capacitive load can change the gain.

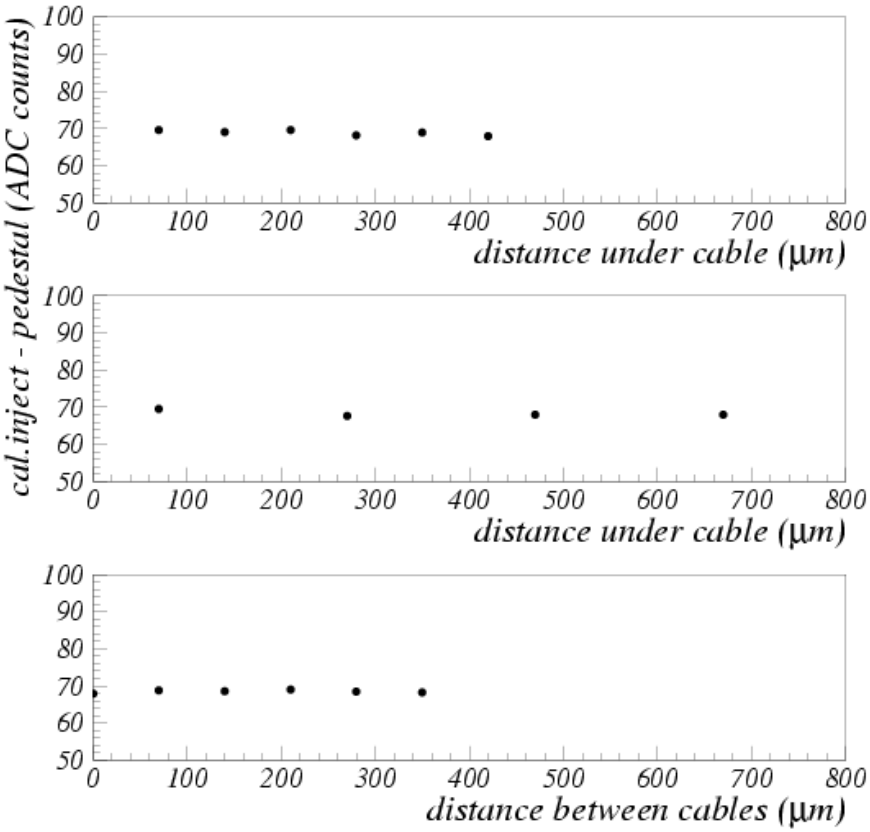
ADC counts after pedestal subtraction by cal_inject

	BW=0	BW=1	BW=2	BW=4	BW=6	BW=8	BW=15
No load	75.5	76.4	75.1	75.9	76.0	74.3	75.4
cable only	77.5	77.9	76.9	74.7	71.5	71.0	58.0
Sensor 70V	76.3	73.8	71.9	65.6	64.4	64.2	46.5
Sensor 0V	72.5	69.0	67.3	60.4	53.8	53.8	39.0

We are using BW=4 for our most of the tests.

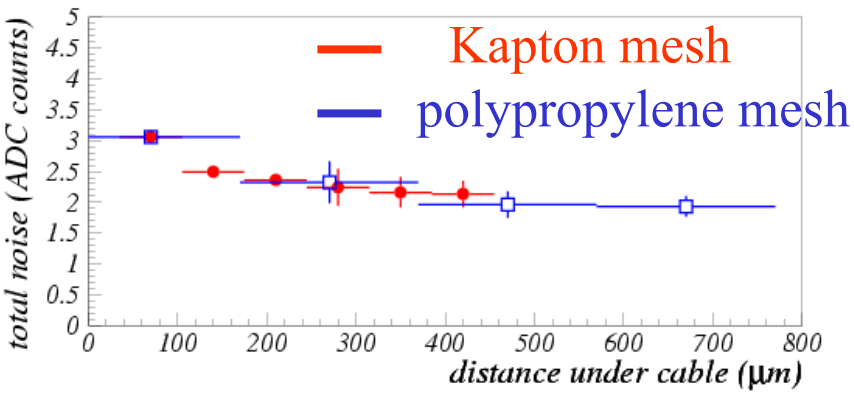
Checking Gain (cont'd)

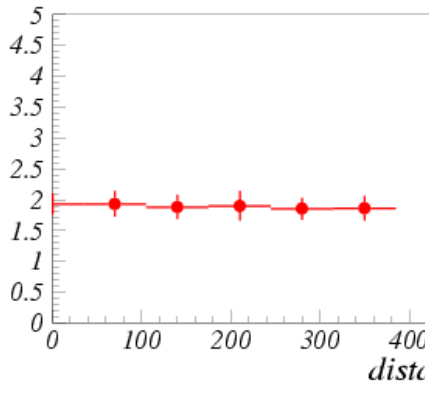
- Measure both gain by cal_injection and noise at the same time for the chip bonded only cable. (BW=6)



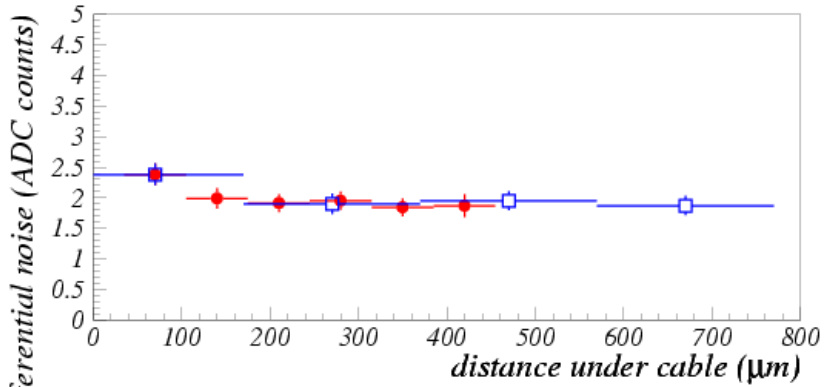
- No change of the gain. ➔ ADC counts is a good measure for noise.

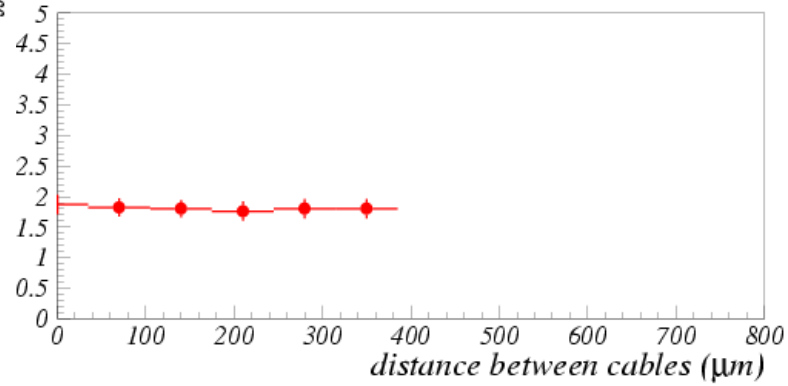
Mystery





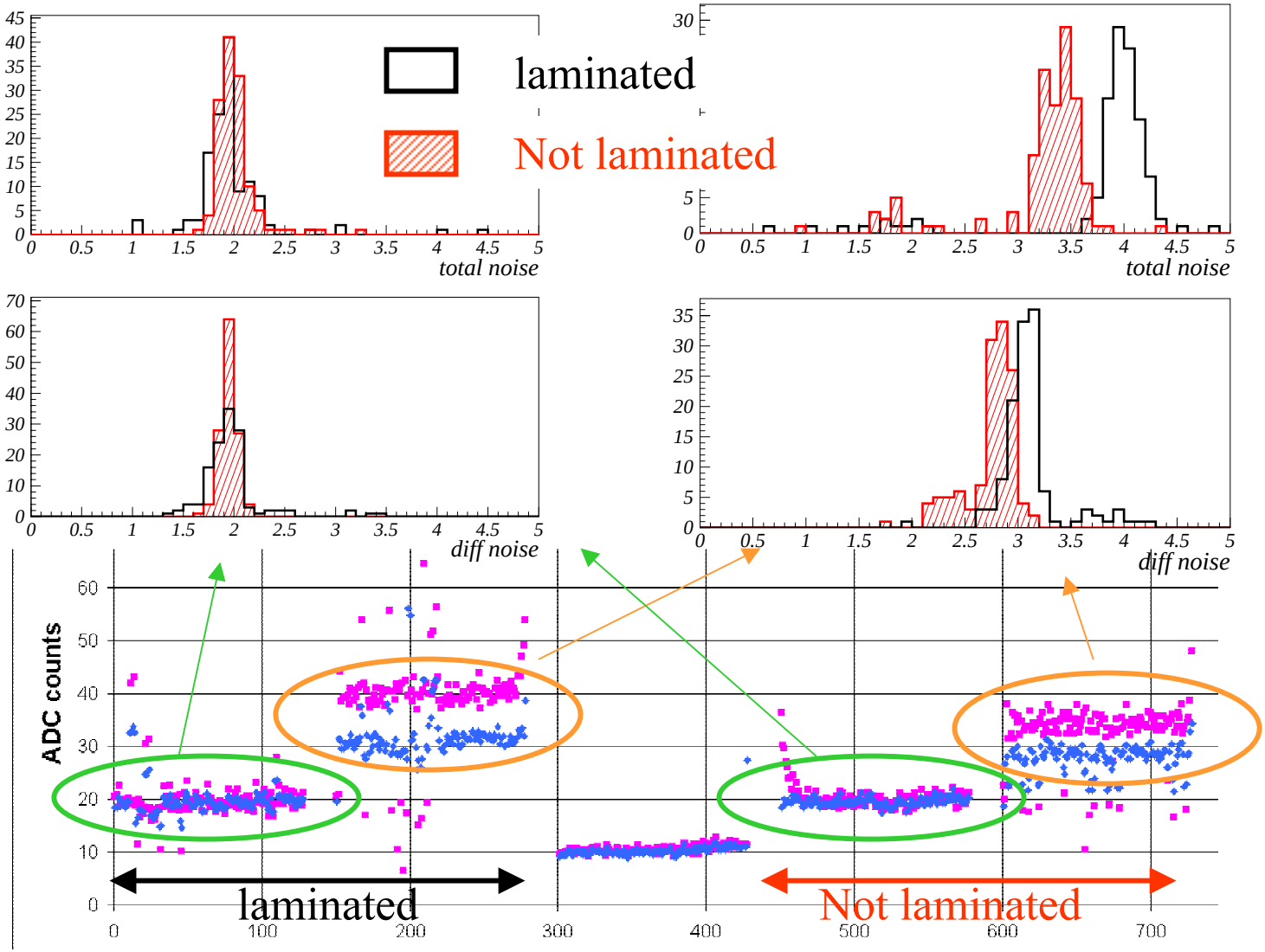
600μm polypropylene mesh plus 70μm Kapton sheet between the bottom cable and grounding plane





- Pick-up noise from the ground plane (common mode noise) is observed. ← 500μm separation may be needed.
- We never see the noise increase due to the proximity of eacg cable. ← WHY????????????

Laminated vs Non-laminated cable



- No difference can be seen for the cable part.

New versions of SVX4

- 11 Wafers in hand. (~10(?) chips are diced.)
- After wafer probing, large number of chips will be diced, probably in two or three weeks.
- Both version A and B work.
- Both D0 and CDF mode work.
- Pedestal slope across the channels has almost gone, less than one ADC count level. But this depends on the gain. Need gain measurement for quantitative estimates.
- Channel to channel variation significantly reduced.
- Small pipeline cell dependence of pedestal still exists ← can be eliminated by RTPS in principle)
- Faster comparator gives us 10 or 20 ADC counts of pedestal.
- Other basic functions are confirmed to work. (sparsification, RTPS, etc.)